	Ref #	Hits	Search Text	DBs	Time Stamp
1	S1	177034	(simulat$ or emulat$)	USPAT	2004/12/23 10:26
2	S2	2293911	(bidirection$ or ((two adj2 way) or inout or duplex)) near$3 (wire or line)	USPAT	2004/12/22 15:54
3	S3	14702	S1 with S2	USPAT	2004/12/22 15:55
4	S5	5	S4 same (control$ or detect$ or compar$) same (change or value)	USPAT	2004/12/22 15:57
5	S6	5	S3 same (Verilog and VHDL)	USPAT	2004/12/22 16:04
6	S4	107	S3 same (port or node) same (path or loop or mesh)	USPAT	2004/12/22 16:59
7	S7	1	("6480817").PN.	USPAT	2004/12/22 16:50
8	S8	21	("4488354" | "4683384" | "4744084" | "4791357" | "4821173" | "4942317" | "4978633" | "4980889" | "5105373" | "5166937" | "5300835" | "5317698" | "5406147" | "5426591" | "5426739" | "5428750" | "5452229" | "5479123" | "5481484" | "5535223" | "5572437").PN.	US-PGPUB; USPAT; USOCR	2004/12/22 16:51
9	S9	2	(US-5428750-$ or US-5300835-$).did.	USPAT	2004/12/22 16:58
10	S10	0	wire with timing with I/O with model	USPAT	2004/12/22 17:00
11	S11	2968	wire with model	USPAT	2004/12/22 17:00
12	S12	32	S11 with timing	USPAT	2004/12/22 17:02
13	S14	27	timing with annotation with wire	USPAT	2004/12/23 10:38
14	S15	57	model with wire with delay	USPAT	2004/12/23 13:37
15	S16	0	characterize with wire with delay	USPAT	2004/12/23 11:25
16	S17	4	(model with wire).ti.	USPAT	2004/12/23 11:28
17	S18	1	(US-6763503-$).did.	USPAT	2004/12/23 11:30
18	S19	9	("5610833" | "5629860" | "5694344" | "5706206" | "6175947" | "6189131" | "6243653" | "6291254" | "6381730").PN.	US-PGPUB; USPAT; USOCR	2004/12/23 13:50
19	S20	1	((wire or path or line) adj (load or delay) adj (simulate$ or emulate$ or model)) same verilog	USPAT	2004/12/23 13:42
20	S21	129	wire adj model	USPAT	2004/12/23 13:42
21	S22	11	S21 same simulat$	USPAT	2004/12/23 13:43
22	S23	32	wire adj load adj model	USPAT	2004/12/23 13:46
23	S24	1	annotate with path with delay	USPAT	2004/12/23 13:46
24	S26	66	verilog and tran	USPAT	2004/12/23 13:53
25	S27	4	(interconnect adj2 model$) same load same delay	USPAT	2004/12/23 16:42
26	S28	315	(interconnect adj2 model$)	USPAT	2004/12/23 16:42
27	S29	10	S28 with path	USPAT	2004/12/23 16:43
28	S30	1	NN9012277	DERWENT; IBM_TDB	2004/12/27 10:32
29	S41	52	half adj duplex adj modem	USPAT	2004/12/27 10:55
30	S42	1	"5999734".pn.	USPAT	2004/12/27 10:56
31	S43	1	"6496955".pn.	USPAT	2004/12/27 10:57
32	S44	1	"6584598".pn.	USPAT	2004/12/27 10:58
33	S45	3184	simulat$ same wire	USPAT	2004/12/27 10:58
34	S46	1377	simulat$ with wire	USPAT	2004/12/27 10:58
35	S47	66	S46 with model	USPAT	2004/12/27 11:02

36	S48	0	S47 same verilog	USPAT	2004/12/27 10:59
37	S49	4	S47 same load	USPAT	2004/12/27 10:59

	Ref #	Hits	Search Text	DBs	Time Stamp
38	S50	20	model same (I/o near pad)	USPAT	2004/12/27 11:13
39	S51	2	("6480817").URPN.	USPAT	2004/12/27 11:07
40	S52	21	("4488354" | "4683384" | "4744084" | "4791357" | "4821173" | "4942317" | "4978633" | "4980889" | "5105373" | "5166937" | "5300835" | "5317698" | "5406147" | "5426591" | "5426739" | "5428750" | "5452229" | "5479123" | "5481484" | "5535223" | "5572437").PN.	US-PGPUB; USPAT; USOCR	2004/12/27 11:07
41	S53	49	verilog near model	USPAT	2004/12/27 11:14
42	S54	0	S53 near wire near load	USPAT	2004/12/27 11:15
43	S60	1	"20040162711"	US-PGPUB; USPAT	2004/12/27 14:05
44	S61	1	1997GB-0024259	US-PGPUB; USPAT; DERWENT	2004/12/27 14:37
45	S63	45	(bi-directional with buffer).ti.	US-PGPUB; USPAT; DERWENT	2004/12/27 15:36
46	S64	1	1996KR-0018252	DERWENT	2004/12/27 14:39
47	S65	7229	port same programming	US-PGPUB; USPAT; DERWENT	2004/12/27 15:20
48	S66	72	S65 and HDL	US-PGPUB; USPAT; DERWENT	2004/12/27 15:20
49	S67	2	S66 and (change same detection)	US-PGPUB; USPAT; DERWENT	2004/12/27 15:22
50	S68	248	HDL same port	US-PGPUB; USPAT; DERWENT	2004/12/27 15:22
51	S69	8	S68 and path and (change same detection)	US-PGPUB; USPAT; DERWENT	2004/12/27 15:25

	Ref #	Hits	Search Text	DBs	Time Stamp
52	S70	9226	HDL	US-PGPUB; USPAT; DERWENT	2004/12/27 15:25
53	S71	216	HDL same path	US-PGPUB; USPAT; DERWENT	2004/12/27 15:26
54	S72	34	S71 and port and matching	US-PGPUB; USPAT; DERWENT	2004/12/27 15:27
55	S73	43	HDL and (Bus adj functional adj Model)	US-PGPUB; USPAT; DERWENT	2004/12/27 15:27
56	S74	446	HDL and Channel and (bus or path) and port	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2004/12/27 15:38
57	S75	21	S74 and (detection same change)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2004/12/27 15:41
58	S76	121	HDL same channel	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2004/12/27 15:43

	Ref #	Hits	Search Text	DBs	Time Stamp
59	S77	0	HDL same (channel with bi-directional)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2004/12/27 16:04
60	S78	8	crosspoint with NMOS	USPAT	2004/12/28 16:03
61	S81	227	703/25.ccls.	USPAT	2004/12/28 15:48
62	S83	7	S81 and verilog	USPAT	2004/12/28 15:48
63	S85	2	NMOS with verilog	USPAT	2004/12/29 10:06
64	S86	362	virtual with port with connection	USPAT	2004/12/29 10:06
65	S87	1	S86 with directional	USPAT	2004/12/29 13:42
66	S88	0	S86 with signal with integrity	USPAT	2004/12/29 10:09
67	S89	21	S86 with signal	USPAT	2004/12/29 10:10
68	S90	3	timing with propogation with delay	USPAT	2004/12/29 13:55
69	S91	28458	timing with delay	USPAT	2004/12/29 13:46
70	S92	258	timing with delay with port	USPAT	2004/12/29 13:48
71	S93	71	S92 same (simulat$ or emulat$ or model$ or process$ or execut$)	USPAT	2004/12/29 13:53
72	S94	2	S93 and NMOS	USPAT	2004/12/29 13:53
73	S96	1402	annotate timing with simulat$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2004/12/29 14:32
74	S100	37	S96 and verilog	USPAT	2004/12/29 14:01
75	S101	49	timing adj report	USPAT	2004/12/29 14:25
76	S102	195	input and port adj delay	USPAT	2004/12/29 14:26
77	S103	180	input adj2 port adj2 delay	USPAT	2004/12/29 14:29
78	S104	76	input adj2 port adj delay	USPAT	2004/12/29 14:31
79	S106	145	verilog and HDL and (timing with delay)	USPAT	2004/12/29 14:49
80	S107	169	verilog and vHDL and (timing with delay)	USPAT	2004/12/29 14:49
81	S108	501	verilog and media	USPAT	2004/12/30 16:12
82	S109	1	S108 and CDROM	USPAT	2004/12/30 16:14
83	S110	179	S108 and disks	USPAT	2004/12/30 16:14
84	S111	38	verilog same media same disk$	USPAT	2004/12/30 16:16

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	US 4963863 A	19901016	7	Broadband signal switching equipment	340/2.29	
2	US 5396435 A	19950307	12	Automated circuit design system and method for reducing critical path delay times	716/6	703/19; 716/18
3	US 5428750 A	19950627	20	Bi-directional buffers for mounting a plurality of integrated circuit devices	710/305	710/100
4	US 6442738 B1	20020827	8	RTL back annotator	716/5	716/18; 716/6
5	US 6496955 B1	20021217	20	Latch mapper	716/3	703/27; 716/18; 716/5; 716/7
6	US 6553338 B1	20030422	10	Timing optimization in presence of interconnect delays	703/14	703/15; 703/19; 716/6
7	US 6587999 B1	20030701	7	Modeling delays for small nets in an integrated circuit design	716/6	716/10; 716/17; 716/18; 716/5
8	US 6751744 B1	20040615	13	Method of integrated circuit design checking using progressive individual network analysis	713/401	716/10; 716/5; 716/6
9	US 6763503 B1	20040713	7	Accurate wire load model	716/4	716/10; 716/5
10	US 6789212 B1	20040907	28	Basic cell for N-dimensional self-healing arrays	714/9	714/12; 714/3